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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/976,004	PHADNIS ET AL.	
	Examiner	Art Unit	
	Robert W. Wilson	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 2-7-02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 28-29, 81-82, 112-113, and 142-143 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Referring to claims 28, 81, 112, & 124; what is meant by "wherein said second information element comprises a non-mandatory information element according to a signaling specification used for signaling in said ATM network, wherein non mandatory information elements can be ignored by said plurality of switches when processing signaling message according to said signaling specification?"

Referring to claim 142, what is meant by "mandatory information elements and a non-mandatory information element according to a signaling protocol.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 28-29, 81-82, 112-113, 142-143 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention..

Referring to claims 28, 81, 112, & 124; where in the applicant's specification, UNI spec., or NNI specification are the details about mandatory information elements and non-mandatory information elements taught? Where in the applicant's specification, UNI spec., or NNI specification are the details about how non-mandatory information elements are ignored?

Referring to claim 142, where in the applicant's specification, NNI specification, or UNI specification are "mandatory information elements and a non-mandatory information element" processing described as how and when they should be ignored?

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 24, 30-35, 79-80, 85-91, 95, 99-103, 107-110, 114-118, 122-123, 127-129, 135, 139, & 140 are rejected under 35 U.S.C. 102(e) as being anticipated by Gupta (U.S. Patent No.: 6,278,714).

Referring to claim 24, Gupta teaches: a device (The Control Point Processor (210 per Fig 2) contains a Controlling Device (Fig 3B) (device) per col. 5 line 22 to col. 6 line 32) setting up virtual circuits (setting up a Virtual Circuit Bunch (VCB) per col. 12 lines 40 to 56 and per Fig 16) between a first end system (node A per Fig 1) and a second end system (node J per Fig 1), said virtual circuits setup on a network connecting said first end system to said second end system (The plurality of VCs are setup on an ATM network which interconnects node A and node J per col. 12 line 40 to 56) said device (The Control Point Processor (210 per Fig 2) contains a Controlling Device (Fig 3B) (device) per col., 5 line 22 to col. 6 line 32) comprising:

An outbound interface coupled to said network (COMMUNICATIONS PORT (385 per Fig 3B) is the outpoint interface coupled to the ATM network per col. 4 line 54 to col. 5 line 5)

A message construction block coupled to said outbound interface (CPU (355 per Fig 3B) is the message construction block which is coupled to the COMMUNICATIONS PORT (385 per Fig 3B) (outbound interface) per col. 6 lines 48 to 64) and

A call control logic for causing said message construction block to construction a first signaling message requesting said a first virtual circuits to be set up and to send said first signaling message on said network to said second end system (The CPU (355 per Fig 3B) has control logic for causing the CPU (355 per Fig 3B) to construct a first signaling message (Figs 7A, 7B, or 7C

per col. 8 line 9 to 49) to be set up and sent on the ATM network to node B (2nd end system) per col. 12 line 40 to 56);

wherein said first end system (Node a per Fig 1) is a first ATM switch (col. 5 line 3), said second end system (Node B per Fig 1) is a second ATM switch (col. 5 line 3) and said first signaling message (Fig 7A, 7B, 7C) is a single signaling message (col. 8 line 8 to 49) and said network is ATM network (col. 5 line 3)

wherein said first signaling message is a single message ,wherein a first information element is designed to request set of single virtual circuit comprised in said first plurality of virtual circuits and a second information element is designed to request set of a second virtual circuits comprised in said plurality of virtual circuits (Figure 7A-7C and per col. 8 lines 8 to 63 show a single signaling message which have multiple information element (2nd information element) associated with a plurality of virtual circuits)

an inbound interface designed for receiving on said ATM network a first acceptance message indicating that only said single virtual circuit setup if any of the plurality of switches in a connection path between said first end system and said second end system is designed not to support setting up said plurality of virtual circuits in response to said single signaling message, wherein said first acceptance message is received in response to sending said first signaling message to said second end system (Communication Port (385 per Fig 1) receives an ACK per col. 7 lines 1-8 which the examiner interprets as indicating what circuits can be setup and would only set up a single circuit if it was available which would include not being designed to support the plurality wherein Figure 7A & 7B represents the single signaling message)

a parser designed for examining said first acceptance message and forward said first acceptance message to said call control logic (The CPU per Fig 3B performs the function of the parser the ACK and internally forwarding the ACK to inherent control logic for examination)

Regarding claim 30 wherein said call control logic causes said message construction block to send a second signaling message to said single as said signal signaling message requesting set up of a second plurality of virtual circuits wherein said inbound interfaced designed for receiving a second acceptance message also as a single message said second acceptance message indicating that said plurality of switches in a connection path between said first ATM switched and said second ATM switch have set up said second plurality of virtual circuits (385 per Fig 1 (inbound interface) receives inherent 2nd VCB or second signaling message per Fig 16 inherent second ACK or second signaling response per Fig 16)

Regarding claim 31, wherein said plurality of switches accept said second plurality of virtual circuits but immediately provision fewer than second plurality of virtual circuits wherein the specific ones of said second plurality of virtual circuits accepted but not provision from a set of inactive virtual circuits wherein said call control logic is design to cause said message construction block to send a third signaling message to activate at least one of said set of inactive

virtual circuits (VCs are assigned in table but without traffic (provisioning fewer) per col. 8 lines 8 to 32. Figure 17 shows request or third signaling message to activate VC which are in the table)

Regarding claim 32, wherein said plurality of virtual circuits is treated as a group of virtual circuits wherein said first ATM switch and said second ATM switch support a plurality of groups including said group and said device further comprising a memory for storing a bundle structure associated with each of plurality groups wherein said bundle structure store information identifying the specific plurality of virtual circuits forming the corresponding group (360 or 365 per Fig 1 (memory) are capable of storing table of Fig 8B)

Regarding claim 33, wherein said memory is designed storing a plurality of call reference structures and a plurality of per-VC structures, wherein each of said plurality of call reference structure maintains the state of a call wherein signaling message related to each group are received on a corresponding call and wherein each per-vc structure stores information related to a plurality of call parameters accepted for a corresponding one of said plurality of virtual circuits (The memory previously cited is capable of storing Figure 8a & 8B (call reference structure) which maintain call state)

Regarding claim 34, wherein each design comprises s switch in said connection path said memory is further designed for storing a plurality of switch structures wherein each of said plurality of switch stores a mapping of an identifier of each virtual circuit in bound direction to another identifier of a virtual circuit in outbound direction (Fig 6 shows forwarding table and reverse table (memory) with separate VCIs associated with each respectively)

Regarding claim 35, wherein said first ATM switch comprises an edge router (A1 per Fig 1) said signaling message contains a bundle identifier which is propagated without translation by aid plurality of switches (The signaling message per Fig 7A to 7C contains VCB request field (bundle identifier) which propagate through all of the switches and is unchanged or without translation)

Referring to claims 79, Gupta teaches: a method of setting up virtual circuits between a first asynchronous transfer mode (ATM) switch and a second ATM switch, said plurality of virtual circuits being setup on a ATM network connecting said first ATM switch to said second ATM switch (The Controlling Device (Fig 3B) performs the method of setting up a plurality of virtual circuits (col. 12 line 40 to 56) between a first Asynchronous Transfer Mode Switch (node A per Fig 1) and a second Asynchronous Transfer Mode Switch (node B per Fig 1), said plurality of virtual circuits setup on a network connecting said first ATM switch to said second ATM switch (The plurality of VCs are setup on an ATM network col. 5 line 2 which interconnects node A (first Asynchronous Transfer Mode Switch) and node J(second Asynchronous Transfer Mode Switch) per col. 12 lines 40 to 56) said method comprising:

Sending on said ATM network to said second ATM switch a single signaling message requesting a plurality of virtual circuits to be setup (A first signaling message (Fig 7A, 7B, 7B) requesting a plurality of virtual circuits (VCB) per Fig 16 per col. 8 lines 9 to 49) is sent to node B (second ATM switch))

Receiving an acceptance message in response to sending said single signaling message said acceptance message indicating the a plurality of ATM switches (in a connection path between said first ATM switch and said second ATM switch have set up said plurality of virtual circuits in response to said single signaling message (Fig 1 shows in connection path between said first ATM switch (A per Fig 1) and said second ATM switch (B per Fig 1) have set up said plurality of virtual circuits receives ACK per Fig 17 per col. 7 lines 1 to 8 (acceptance message)

Wherein said plurality of ATM switches accept said plurality of virtual circuits but immediately provision fewer than said plurality of virtual circuits (VCs are assigned in table based upon what is available or fewer than requested per col. 8 lines 8 to 32) wherein the specific ones of said plurality of virtual circuits accepted but not provisioned from a set of inactive virtual circuits which cannot be used (Circuits are setup or provisioned per Fig 16 do not carry traffic)

Sending a second signaling message to complete provisioning of at least one of set of inactive virtual circuits (sends request (2^{nd} signal) per Fig 17 per col. 12 line 57 to col. 13 line 17)

In Addition Gupta teaches:

Regarding claim 80, wherein said acceptance message is received only if each of said plurality of ATM switches is designed to set up of said plurality of virtual circuits in response to said single signaling message, wherein said single signaling message comprises a plurality of information elements wherein a first information element is designed to request set up of a single virtual circuit and a second information element is designed to request set up of a second virtual circuits comprising a plurality of virtual circuits in response to said single signaling message (VCB request per Fig 16 or single signaling message (Fig 7A to 7C) which contains a plurality of information element)
Receiving another acceptance message that only a single message indicating only a single virtual circuit is provisioned if any of a plurality of switches in a connection path is designed not to support set up of said plurality of virtual circuits (receives ACK per col. 7 lines 1 to 8 (2^{nd} acceptance message) to the single signaling message (Fig 7A to 7C) when VC cannot be supported)

Regarding claim 85, wherein said fewer than said plurality of virtual circuits corresponds to one virtual circuit such that only one virtual circuit is provided in response to said single signaling message even when said plurality of switches have set up said plurality of virtual circuits in response to said single signaling message and said acceptance message is received by said first ATM (The reference teaches sending a single message per Fig 7B in which only in a plurality of VCs which are available will be stored in the tables per col. 12 line 47 to col. 14 line 13;

however, one of the ACK received back between switches can indicate only a single VC has been set up)

Regarding claim 86, wherein said sending is performed from one of said first ATM system or said plurality of ATM switches (Message is sent from CP which can represent a plurality of ATM switches per col. 5 line 3 and col. 5 lines 54 to 67)

Regarding claim 87, wherein said plurality of virtual circuits (720B1 & 730Bn per Fig 7A) is treated as a group of virtual circuits (710 per Fig 7A) wherein said first ATM switch (Node A per Fig 1) and said second ATM switch (node J per Fig 1) support a plurality of groups (Plurality of 710 per Fig 7A) including said group (710 per Fig 7A0 said method further comprising maintaining a bundle structure (Table as shown in Fig 8B) associated with each of said plurality of groups (Different VCBs per Fig 8B) wherein the bundle structure (Table per Fig 8B) stores information identifying the specific plurality of virtual circuits (Port (VCI) per Fig 8B) identifying the specific plurality of virtual circuits (VCIs per Fig 8B) forming the corresponding group (VCB # (group) per Fig 8B)

Regarding claim 88, further comprising maintaining a plurality of call reference structures, wherein signaling messages related to each group are received on a corresponding call (Fig 8B is the call reference structure which maintains the state of assignments corresponding to a call in a table structure.) and maintaining a plurality of per-VC structure, wherein each per-VC structure store information relate to a plurality of call parameters accepted for a corresponding one of said plurality of virtual circuits (A table is maintain which stores the PORT (VCI), VCB, NEXT NODE VCB, & Destination per Fig 8A or VC-structure which has information related to VCB and DESTINATION which were call parameters per Fig 7B)

Regarding claim 89, wherein said sending and receiving and each of said maintaining are performed in a switch contained in said connection path said (Each node A thru node J which are in the connection path per Fig 1 send, receives, and maintains a tables per Fig 6 and 7B) said method further comprising:
maintaining a plurality of switch structures, wherein each of said plurality of switch structures stores a mapping of an identifier of each of said virtual circuit in inbound interface in inbound direction to another identifier of the virtual circuit in outbound direction (Additionally each switch has a forwarding table which maps the VCI # identifier of each virtual circuit in inbound direction (Forwarding per Fig 6) and another identifier (VCI#) of each said virtual circuit in outbound direction (Reverse per Fig 6) using said plurality of switches (nodes per Fig 1)

Regarding claim 90, wherein said first ATM switch (node A per Fig 1 is an edge router (switch on edge or network per Fig 1) wherein a signaling message (Fig 7B contains a bundle identifier (VCB REQUEST per Fig 7A) which is propagated without translation by each of said plurality of switches (nodes per Fig 1) (The nodes do not change the VCB Request field)

Regarding claim 91, wherein said plurality of virtual circuits comprise a switched virtual circuit (Virtual circuit bunch or plurality of virtual circuits are set up between switches thus switched virtual circuit per col. 8 line 9 to col. 9 line 20)

Referring to claim 95, Gupta teaches: a method of supporting setting up of virtual circuits between a first asynchronous transfer mode (ATM) switch and a second ATM switch, said virtual circuits being setup on a ATM network connecting said first ATM switch to said second ATM switch (The Controlling Device (Fig 3B) in node J supports the method of setting up a plurality of virtual circuits (set-up VCB per col. 12 lines 40 to 56) between a first Asynchronous Transfer Mode Switch (node A per Fig 1) and a second Asynchronous Transfer Mode Switch (node J per Fig 1), said plurality of virtual circuits terminating on the first ATM switch and said second ATM switch (The plurality of VCs terminate on CP as endpoint per col. 5 lines 66 in node A (first Asynchronous Transfer Mode Switch) and terminate (end point of a VC per col. 5 line 65 to col. 6 line 2 & col. 12 lines 40 to 56) node J (second Asynchronous Transfer Mode Switch)) said method comprising:

Receiving from said first ATM switch on said ATM network a signaling request requesting said virtual circuits to be set up if said plurality of virtual circuits can be set up between said device and said second ATM switch in response to said single signaling request alone (node J (receives) a signaling request per Fig 16 per format per Fig 7A, 7B, or 7C) requesting a plurality of virtual circuits (receives a request per col. 8 lines 9 to 49 for virtual circuits to be setup if they are available)

sending an acceptance message (ACK per col. 9 line 7 to 32) as a response to said single signaling message request said acceptance message indicating that said plurality of virtual circuits are set up if said plurality of virtual circuits (VCB REQUEST per Fig 16 and per Fig 7A, 7B, 7C) can be set up between said device (CP per 2) and said second ATM switch (node J per Fig 1) in response to a single request (Fig 7A, 7B, or 7C) upon receiving ACK per Fig 16 virtual circuits are setup)

provisioning fewer than said plurality of virtual circuits to said second ATM switch before performing said sending (only circuits which are available are set up virtual per col. 8 line 8 to 47) wherein the specific ones of said plurality of virtual circuits which are set up but not provisioned form a set of inactive virtual circuits which cannot be used (Circuits setup are inactive until they are requested per Fig 17) .

In addition Gupta teaches:

Regarding claim 99, receiving a second signal message requesting activation of at least one of said set of inactive virtual circuits (in response to receiving said second signaling message (Request (second message) per Fig 17 per col. 7 line 1 to 26)
Completing provisioning of said at least one of said set of inactive virtual circuits in response to receiving said second signaling message (Fig 17)

sending a completion message in response to said second signaling message said completion message indicating said at least one of said s3et of inactive virtual circuits have been provisioned (ACK per Fig 17 and per col. 7 line 1 to 26)

Regarding claim 100, storing said plurality of parameters associated with said range of virtual circuits and provisioning said range of virtual circuits using said plurality of parameters (Each switch inherently stores and forwards the VCB which has the range of parameters)Provisioning said range of virtual circuits using said plurality of parameters whereby said plurality of parameters are transmitted only once for provisioning said range of virtual circuits (The VCB message is only transmitted once in each switch)
Whereby the parameters are transmitted only once for provisioning said range of virtual circuits (Request is only send once)

Regarding claim 101, wherein said single signal request and second signal message in received in the form of ATM cells (The reference teaches ATM switches so the request and second message are inherently ATM cells)

Regarding claim 102 , wherein said device comprises one of said first ATM switch and said second ATM switch (Node A and Node J are ATM switches)

Referring to claim 103, Gupta teaches: an apparatus for supporting the setting up of virtual circuits between a first ATM switch and a second ATM switch, said virtual circuits being set up on a ATM network connecting said first ATM switch to said second ATM switching said virtual circuits terminating at said first ATM switch and said second ATM switch (Controlling Device (Fig 3B) in node J (Fig 1) (apparatus) for supporting the setting up a plurality of virtual circuits (VCB per col. 12 lines 40 to 56) between node A (First ATM switch) and node J (second ATM switch) the plurality of virtual circuits being set up (VCB setup per col. 12 lines 40 to 56) on an ATM network (col. 5 line 2) connecting node A per Fig 1 (First ATM switch) to node J per Fig 1 (second ATM switch) with the plurality of virtual circuits terminating (The plurality of VCs terminate on CP as endpoint in nodes per col. 5 lines 66) on node A per Fig 1) and node J (second ATM switch) per col. 12 lines 40 to 56)

An in-bound interface for receiving from a first ATM switch on said ATM network a single signaling request requesting a virtual circuits to be set up (Node J (Fig 1) has COMMUNICATIONS PORT (385 PER Fig 3B) (in-bound interface) which is capable of receiving from node A (Fig 1) (First ATM switch) on the ATM network (Fig 1) a single signal request (Fig 7A, 7B, or 7C) requesting said plurality of virtual circuits to be setup (VCB setup per col. 12 lines 40 to 56) wherein said acceptance message is in response to said single signaling message (ACK per Fig 16)

a call control logic (The node J has a CPU per Fig 3B or call control logic) for receiving a single signaling message (Fig 7A, 7B, or 7C) said call control logic receiving VCB request per Fig 16)

sending an acceptance message (ACK per Fig 16) if said plurality of virtual circuits (VCB) can be set up between a device (node) containing said call control logic (CP) and said second ATM switch (node J per Fig 1) in response to said single signaling request (Fig 7A, 7B, or 7C) per col. 12 lines 40 to 56) wherein said acceptance message is sent as response to said single signaling message (ACK per Fig 16)

wherein said acceptance message is sent as a response to said single signaling message (ACK sent in response to VCB request per Fig 16)

wherein said call control logic is for provisioning fewer than said plurality of virtual circuits to said second ATM switch before sending said acceptance message (col. 9 lines 9 to 32) wheiren the specific ones of said plurality of virtual circuits which are set up but not provisioned form a set of inactive virtual circuits which cannot be used (Circuits setup per Fig 16 cannot be used until requested and ACK per Fig 17)

wherein the specific ones of said plurality of virtual circuits which are set up but not provisioned form a set of inactive virtual circuits which cannot be used (Virtual circuits per Fig 16 are inactive and comprise a set which cannot be used until requested per Fig 17)

In Addition Gupta teaches:
Regarding claim 107, wherein said inbound interface is designed to receive a second signaling message requesting activation of at least one said inactive virtual circuits wherein said call control logic is configured to complete provisioning of said at least one of said set of inactive virtual circuits and then to send a completion message indicating said at least one of said set of said inactive virtual circuits has been activated (Fig 17)

Regarding claim 108, wherein said single signaling message contains a plurality of parameters related to a range of virtual circuits comprised in said plurality of virtual circuits said apparatus further comprising a memory storing said plurality of parameters associated with said range of virtual circuits using said plurality of parameters, whereby said plurality of parameters are transmitted only once for provisioning said range of virtual circuits (Fig 7A single signaling message contains a plurality of parameter and range (no of VC) and the values are stored in table per Fig 8B)

Regarding claim 109, comprising one of said first ATM switch said second ATM switch (A & J are ATM switches)

Referring to claim 110, Gupta teaches: a method of setting up a virtual circuits between a first asynchronous transfer mode (ATM) switch and a second ATM switch, said plurality of virtual circuits being setup on a ATM network connecting said first ATM switch to said second ATM switch (The Controlling Device (Fig 3B) performs the method of setting up a plurality of virtual circuits (col. 12 line 40 to 56) between a first Asynchronous Transfer Mode Switch (node A per Fig 1) and a second Asynchronous Transfer Mode Switch (node B per Fig 1), said plurality of

virtual circuits setup on a network connecting said first ATM switch to said second ATM switch (The plurality of VCs are setup on an ATM network col. 5 line 2 which interconnects node A (first Asynchronous Transfer Mode Switch) and node J(second Asynchronous Transfer Mode Switch) per col. 12 lines 40 to 56) said method comprising:

Means for sending on said ATM network to said second ATM switch a single signaling message requesting a plurality of virtual circuits (385 per Fig 3B or means for sending a first signaling message (Fig 7A, 7B, 7B) requesting a plurality of virtual circuits (VCB per col. 8 lines 9 to 49) is sent to node B (second ATM switch) and means for sending (385 per Fig 3B)

means for receiving an acceptance message in response to sending said single signaling message said acceptance message indicting that only said signal virtual circuit is provisioned if any of said plurality of switches in a connection path between said device and said second ATM switch is designed not to support set up of said plurality of virtual circuits in response to said single (385 per Fig 3B is means for receiving an acceptance message. The signaling message (Fig 1) in connection path between said first ATM switch (A per Fig 1) and said second ATM switch (B per Fig 1) have set up said plurality of virtual circuits receives ACK per col. 7 lines 1 to 8 (acceptance message) and means for receiving (385 per Fig 3B)

In Addition Gupta teaches:
Regarding claim 114, Means for receiving another acceptance message in response to said single signaling message said another acceptance message indication that said plurality of switches in a connection path between said device and said second ATM switch have set up said plurality of virtual circuits in response to said single signaling message (385 per Fig 3B) is means for ACK per col. 7 lines 1 to 8 (2^{nd} acceptance message) to the single signaling message (Fig 7A to 7C))

Regarding claim 115, means for sending a second signaling message to activate at least one of aid set of inactive virtual circuits (385 per Fig 3B (means) for receiving another ACK per col. 7 lines 1 to 8).

Regarding claim 116, wherein said plurality of virtual circuits is treated as a group of virtual circuits wherein said first ATM switch and said second ATM switch support a plurality of groups including said group and said device further comprising a memory for storing a bundle structure associated with each of plurality groups wherein said bundle structure store information identifying the specific plurality of virtual circuits forming the corresponding group (360 or 365 per Fig 1 (memory) are capable of storing table of Fig 8B)

Regarding claim 117, wherein said memory is designed storing a plurality of call reference structures and a plurality of per-VC structures, wherein each of said plurality of call reference structure maintains the state of a call wherein signaling message related to each group are received on a corresponding call and wherein each per-vc structure stores information related to a plurality of call parameters accepted for a corresponding one of said plurality of virtual circuits

(The memory previously cited is capable of storing Figure 8a & 8B (call reference structure) which maintain call state)

Referring to claim 118, Gupta teaches: a device for supporting setting up a virtual circuits between a first ATM switch and a second ATM switch, said plurality of virtual circuits being set up on a ATM network connecting said first ATM switch to said second ATM switch , each of said plurality of virtual circuits terminating at said first ATM switch and said second ATM switch, (Controlling Point (210 per Fig 2) (device) for the supporting setting up a plurality of virtual circuits (VCB) between node A (First ATM switch) and node J (second ATM switch) the plurality of virtual circuits being set up on an ATM network (col. 5 line 2) connecting node A per Fig 1 (First ATM switch) to node J per Fig 1 (second ATM switch) with the plurality of virtual circuits (The plurality of VCs terminate on CP as endpoint node A per col. 5 lines 66) terminating on node A per Fig 1) and node J (second ATM switch per col. 12 lines 40 to 56) said device comprising: means for sending an acceptance message if said plurality of virtual circuits can be set up between said device and said second ATM switch in response to said single signaling request alone wherein said acceptance message is sent as a response to said single signaling request (385 PER Fig 3B) (means for sending) within the Control Point which is capable of receiving from node A (Fig 1) (First ATM switch) on the ATM network (Fig 1) a single signal request (Fig 7A, 7B, or 7C) requesting said plurality of virtual circuits (VCB) to be setup on node J (second ATM switch) per col. 12 lines 40 to 56)]

means for providing fewer than said plurality of virtual circuits to said second ATM switch before perform said sending (CPU per Fig 3 or means for providing) wherein the specific one of said plurality of virtual circuits which are set up but not provisioned form a set of inactive virtual circuits which cannot be used

Referring to claims 122; Gupta teaches: a computer readable medium storing one or more sequences of instructions for causing a device to set up a virtual circuits between a first asynchronous transfer mode (ATM) switch and a second ATM switch, said plurality of virtual circuits being setup on a ATM network connecting said first ATM switch to said second ATM switch (The Controlling Device (Fig 3B) performs the method of setting up a plurality of virtual circuits (col. 12 line 40 to 56) between a first Asynchronous Transfer Mode Switch (node A per Fig 1) and a second Asynchronous Transfer Mode Switch (node B per Fig 1), said plurality of virtual circuits setup on a network connecting said first ATM switch to said second ATM switch , wherein execution of said one or more sequence of instructions by one or more processor contained in said device causes (The plurality of VCs are setup on an ATM network col. 5 line 2 which interconnects node A (first Asynchronous Transfer Mode Switch) and node J(second Asynchronous Transfer Mode Switch) per col. 12 lines 40 to 56) said device performing::

Sending on said ATM network to said second ATM switch a single signaling message requesting a plurality of virtual circuits to be set up (A first signaling message (VCB request per Fig 7A, 7B, 7B and Fig 16) requesting a plurality of virtual circuits (VCB per col. 8 lines 9 to 49) is sent to node B (second ATM switch)

Receiving an acceptance message as a response to said single signaling message said acceptance message indicating the a plurality of ATM switches (Fig 1) in connection path between said first ATM switch (A per Fig 1) and said second ATM switch (B per Fig 1) have set up said plurality of virtual circuits in response to said single signaling message receives ACK per col. 7 lines 1 to 8 (acceptance message)

Wherein said plurality of ATM switches accept said plurality of virtual circuits but immediately provision fewer than said plurality of virtual circuits (VCs are assigned in table but without traffic (provisioning fewer) per col. 8 lines 8 to 32
Wherein the specific ones of said plurality of virtual circuits which are set up but not provisioned form a set of inactive virtual circuits which cannot be used (Fig 16)

Sending a second signaling message to complete provisioning of at least one of said set of inactive(ACK per Fig 16 or 2nd signaling message)

In Addition Gupta teaches:

Regarding claim 123, Receiving another acceptance message that only a single message indicating only a single virtual circuit is provisioned if any of said plurality of switches in a single signaling message in a connection path is designed not to support set up of said plurality of virtual circuits setting up of said plurality of virtual circuits in response to receiving said single signaling message (receives ACK per col. 7 lines 1 to 8 (2nd acceptance message) to the single signaling message (Fig 7A to 7C) when VC cannot be supported)

Regarding claim 127, wherein said fewer than said plurality of virtual circuits corresponds to one virtual circuit such that only one virtual circuit is provisioned in response to said first signaling message (360 or 365 per Fig 3B are capable of storing software for performing the method per Fig 16)

Regarding claim 128 switch comprising storing bundle structure associated with plurality of groups wherein said bund structure stores information identifying the specific plurality of virtual circuits forming a corresponding group (360 or 365 per Fig 3B are capable of storing Fig 8B

Regarding claim 129, maintains a plurality of call reference structures, wherein each of said plurality of call reference structures maintains the state of a call wherein signal message related to each group are received on a corresponding call per Fig 8A) and maintaining a plurality of per-VC structures, wherein each per-VC structure stores information related to a plurality of call parameters accepted for ea corresponding one of said plurality of virtual circuits (Fig 8B) which is capable of being stored in 360 or 365 per Fig 3B)

Referring to claim 135, Gupta teaches: a computer readable medium (col. 6 line 48 to 64) storing one or more sequences of instructions (col. 4 lines 7 to 50) for causing
a device to support setting up virtual circuits between a first ATM switch and a second ATM switch, said plurality of virtual circuits being set up on a ATM network connecting said first ATM switch to said second ATM switch , each of said plurality of virtual circuits terminating at said first ATM switch and said second ATM switch, wherein execution of said one or more sequences of instructions by one or more processors contained in said device causes said one or more processors to perform the action (Controlling Point (210 per Fig 2) (device) for the supporting setting up a plurality of virtual circuits between node A (First ATM switch) and node J (second ATM switch) the plurality of virtual circuits being set up on an ATM network connecting node A per Fig 1 (First ATM switch) to node J per Fig 1 (second ATM switch) with the plurality of virtual circuits terminating (The plurality of VCs terminate on CP as endpoint node A per col. 5 lines 66 terminating on node A per Fig 1) and node J (The plurality of VCs terminate on CP as endpoint node J per Fig 1 & per col. 5 lines 66. A CPs (processors) contain RAM which is used to execute the instructions to perform the action per col. 4 line 6 to col. 8 line 49) said device to perform the action of:

Receiving from said first ATM switch on said ATM network a signaling request requesting a plurality of virtual circuits to be set up to a second ATM switch (node J (receives) a signaling request (Fig, 7A, 7B, or 7C) requesting a plurality of virtual circuits (VCB) per Fig 16 per col. 8 lines 9 to 49)

Sending an acceptance message if said plurality of virtual circuits can be set up between said device and said second ATM switch in response to said single signaling request alone wherein said acceptance message is sent as a response to said single signaling request sending an acceptance message (ACK per Fig 16)

Provisioning fewer than said plurality of virtual circuits to said second end system before performing said sending (Fig 16 provisions only those that are available or fewer)

Wherein the specific ones of said plurality of virtual circuits which are set up but not provisioned form a set of inactive virtual circuits (Fig 16)

In Addition Gupta teaches:

Regarding claim 139, further comprising: receiving a second signaling message requesting activation of at least one of said set of inactive virtual circuits (Fig 17) completing provisioning of said at least one of said set of inactive virtual circuits (Fig 17) sending a completion message in response to said second signaling message said completion message indicating said at least one of set of inactive virtual circuits have been activated (ACK per Fig 17)

Sending a completion message indicating said at least one of said not-as-yet provisioned virtual circuits have been activated (col. 7 line 1 to 27 & col. 9 lines 21 to 32)

Regarding claim 140, storing said plurality of parameters associated with the range of virtual circuits and provisioning said range of virtual circuits using said plurality of parameters whereby the plurality of parameters are transmitted only once for provisioning said range of virtual circuits (The VCB request is inherently stored in each node and is only passed once before the VCs are setup and the request contains the range of parameters)

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (U.S. Patent No.: 6,278,714).

Referring to claim 25, Gupta teaches the device of claim 24, and receiving a request for a group of virtual circuits from an application (user node which requires an application to work or application per col. 12 line 41 to 56) and communicating the request to call control logic (The local node parse in Control Point (CP) per Fig 2 has call control logic) wherein said call control logic causes said single signaling message (Fig 7A, 7B, or 7C) to be sent in response to said request (col. 12 lines 41 to 56)

Gupta does not expressly call for: signaling application programming interface (API) receiving the request

Gupta teaches: the CP processing can be implemented in software per col. 5 line 22 to 43

It would have been obvious to one of ordinary skill in the art at the time of the invention because the Gupta teaches that the CP processing can be performed in software to implement the software as an application programming interface because it is a type of software implementation.

9. Claim 26 81-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta (U.S. Patent No.: 6,278,714) in view of the UNI Specification (IDS document of record)

Referring to claim 26, Gupta teaches the device of claim 25 wherein said outbound interface (385 per Fig 3B) sends said single signaling message (Fig 7a) in the form of a plurality of Asynchronous Transfer Mode Cells (control message are exchanged between CPs and have to be ATM cells per col. 6 line 6 and col. 5 line 2) and said device further comprising: an output block to generate said message construction block to generate said single signal message which is coupled to said outbound interface (The CPU (355 per Fig 3B) has control logic for causing the CPU (355 per Fig 3B) to construct a single signaling message (Fig 7B) which is coupled to 385 per Fig 3B (outbound interface) per col. 5 line 33 to col. 8 line 49.
5.
Gupta does not expressly call for: a signaling ATM adaptation layer (SAAL) output block to encapsulated and generate the signal message as well as being coupled to the outbound interface.

The UNI specification teaches: set up message for ATM VCs are encapsulated using ATM adaptation layer (SAAL) which is used to generate the signal message per Para 4.1 Pg 35.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the SAAL encapsulation layer which would have to be coupled to the output interface in order to work of UNI specification to the device of Zendle in order to build a system which is standards compliant which will interoperate with legacy standards based systems.

10. Claim 36-37 & 92-93 str rejected under 35 U.S.C. 103(a) as being unpatentable over

Gupta (U.S. Patent No.: 6,278,714) in view of Spiegel (US Patent No.: 5,649,108)

Referring to claim 36, Gupta teaches the device of claim 30 and a signaling message

Gupta does not expressly call for: a common format comprising an acceptance message

Spiegel teaches: a common format comprising an acceptance message per Fig 3 & per col. 5 line 63 to col. 6 line 7.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the common format of Spiegel in place of the two separate message of Gupta so that each switch along the path knows the detailed status of acceptance.

In addition Gupta teaches:

Regarding claim 37, wherein said format allows a range of virtual circuits to be specified, said format further allowing a plurality of traffic parameters to be specified for all of said range of virtual circuits wherein said plurality of parameters in said single signal message specify the

desired parameters and said plurality of parameter in said acceptance message are specified.(Fig 7A is the single message)

Referring to claim 92, Gupta teaches the method of claim 84 and a signaling message

Gupta does not expressly call for: a common format comprising an acceptance message

Spiegel teaches: a common format comprising an acceptance message per Fig 3 & per col. 5 line 63 to col. 6 line 7.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the common format of Spiegel in place of the two separate message of Gupta so that each switch along the path knows the detailed status of acceptance.

In addition Gupta teaches:

Regarding claim 93, wherein said format allows a range of virtual circuits to be specified, said format further allowing a plurality of traffic parameters to be specified for all of said range of virtual circuits wherein said plurality of parameters in said single signal message specify the desired parameters and said plurality of parameter in said acceptance message are specified.(Fig 7A is the single message)

Regarding claim 94, further comprising sending a release message requesting relate of another range of virtual circuits (breakdown request or release per col. 13 line 17 to 29)

Referring to claim 132, Gupta teaches the computer readable medium of claim 122 and a signaling message

Gupta does not expressly call for: a common format comprising an acceptance message

Spiegel teaches: a common format comprising an acceptance message per Fig 3 & per col. 5 line 63 to col. 6 line 7.

It would have been obvious to one of ordinary skill in the art at the time of the invention to add the common format of Spiegel in place of the two separate message of Gupta so that each switch along the path knows the detailed status of acceptance.

Response to Amendment

13. The applicant requested an interview to discussed issues via oral arguments. The examiner agreed to review faxed written arguments. After further consideration the examiner

came to the conclusion there were too many 112/1st and 112/2nd issues to be resolved in an interview and that all of the arguments need to be provided in writing on the record. The examiner subsequently called the applicant an informed the applicant recommendations as to what need to be provided to overcome the 112/1st and 112/2nd rejections (See interview summary for details). It was the examiner opinion that there were too many issues to be resolved in an interviewed that prosecution was best served by recording all of the issues on the record.

112/1st Argument

The examiner respectfully disagrees with the applicant's argument that one of ordinary skill in the art at the time of the invention would know what mandatory and non-mandatory information elements are in the UNI, NNI, or signaling specification. The applicant has not provided any not provided any evidence such or a afidavit from one of ordinary skill in the art so this argument is not persuasive. The applicant has not defined where in the applicant's specification or UNI specification or NNI specification where the mandatory or non-mandatory information elements are processed and how and when they are ignored.

112/2nd
The examiner respectfully disagrees with the applicant's argument that " wherein said second information element comprises non-mandatory information" or one of ordinary skill in the art at the time of the invention would know what this means based upon the UNI or NNI or signaling specification. The examiner cannot find in the specifications where mandatory or non-mandatory are defined so the examiner does not know what this limitation means.

Art Rejection
The examiner respectfully disagrees with the applicant argument that the reference Gupta does not teach: single message request multiple virtual circuit to be set up is send and accepted message indicating that only a single virtual circuit is set up if any of the switches is not designed to support setting up a requested multiple virtual circuit

Gupta teaches: single message request multiple virtual circuit to be set up is send and accepted message indicating that only a single virtual circuit is set up if any of the switches is not designed to support setting up a requested multiple virtual circuit (Figure 16 shows a request for a VCB (multiple virtual circuit) in a single message request. Each switch passed on the message and provide a response back in ACK to predecessor switch as to which circuits are available or switch is designed to support)

The examiner respectfully disagrees with the applicant's argument that the reference Gupta does not teach: said first acceptance message is received in response to sending said first signal message to said second end system

Gupta teaches: said first acceptance message is received in response to sending said first signal message to said second end system (Ack or first acceptance message is received in response to VCB or first signaling message per Fig 16)

The examiner disagrees with the applicant's argument that the reference Gupta does not teach "providing a response to sending message when switch not designed to support"

Gupta teaches "providing a response to sending message when switch not designed to support" Figure 16 shows a request for a VCB (multiple virtual circuit) in a single message request. Each switch passed on the message and provide a response back in ACK to predecessor switch as to which circuits are available or switch is designed to support)

Claim Rejections - 35 USC § 112

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert W. Wilson whose telephone number is 571/272-3075. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571/272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert W. Wilson

Robert W Wilson
Examiner
Art Unit 2619

RWW
12/19/072

Continuation of Disposition of Claims: Claims pending in the application are 24-26,28-37,79-82,85-95,99-103,107-110,112-118,122-124,127-129,135,139,140,142 and 143.

Continuation of Disposition of Claims: Claims rejected are 24-26,28-37,79-82,85-95,99-103,107-110,112-118,122-124,127-129,135,139,140,142 and 143.